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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,971	03/26/2004	Myunghee Lee	10030869-1	7901

57299 7590 11/29/2007

Kathy Manke
Avago Technologies Limited
4380 Ziegler Road
Fort Collins, CO 80525

EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2613	

NOTIFICATION DATE	DELIVERY MODE
11/29/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

avagoip@system.foundationip.com
kathy.manke@avagotech.com
scott.weitzel@avagotech.com

Office Action Summary	Application No.	Applicant(s)	
	10/809,971	LEE ET AL.	
	Examiner	Art Unit	
	David S. Kim	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 7-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Doh et al. (EP 1 187 373 A2, hereinafter "Doh").

Regarding claim 7, Doh discloses:

A method for receiving an optical signal, comprising:

converting (e.g., 11 in Fig. 1) the optical signal into a corresponding current signal;

converting the corresponding current signal into a corresponding voltage signal with a transimpedance amplifier circuit (e.g., 12);

extracting clock information from the corresponding voltage signal (e.g., 15); and

regenerating the corresponding voltage signal to reduce jitter (regeneration of signal and suppression of jitter in paragraph [0002]).

Regarding claim 8, Doh discloses:

A method as in claim 7, further comprising:

compensating for attenuation (e.g., amplifier 13) in the corresponding voltage signal, prior to extracting clock information.

Regarding claim 9, Doh discloses:

A method as in claim 8, wherein the transimpedance amplifier (transimpedance amplifier in paragraph [0003]) has a first frequency response (frequency response of some kind is inherent).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1-2 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable by Doh et al. (EP 1 187 373 A2, hereinafter "Doh") in view of Kim et al. ("CMOS optical receiver chipset for gigabit Ethernet applications", hereinafter "Kim").

Regarding claim 1, Doh discloses:

An optical receiver, comprising:

a photodetector (e.g., 11 in Fig. 1) receiving an optical signal and generating a corresponding current signal;

a gain stage (e.g., 12 and 13) coupled to the photodetector receiving the corresponding current signal and converting it to a corresponding voltage signal; and

a clock data recovery (CDR) circuit (e.g., 15) directly coupled to the gain stage receiving the corresponding voltage signal, extracting clock information from the corresponding voltage signal, and regenerating the corresponding voltage signal to reduce jitter (suppression of jitter in paragraph [0002]).

Doh does not expressly disclose:

said gain stage being a ***transimpedance amplifier circuit (TIA)*** *so that a TIA is coupled to the photodetector and so that the CDR is directly coupled to the TIA* (emphasis Examiner's).

However, such a TIA is known in the art, as shown by Kim (Fig. 1(b)). Notice that Kim suggests a modification from one optical receiver apparatus in Fig. 1(a) to another optical receiver apparatus in Fig. 1(b). Also, notice that Fig. 1(a) in Kim corresponds closely with Fig. 1 in Doh. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to provide a similar modification to the optical receiver apparatus in Fig. 1 of Doh, e.g., removal of limiting amplifier 13. One of ordinary skill in the art would have been motivated to do this to reduce apparatus complexity, resulting in low power, small size, and low cost (Kim, p. I-29, col. 1, last paragraph). In view of such a modification, the optical receiver of Doh in view of Kim would comprise the TIA of the claim.

Regarding claim 2, Doh in view of Kim discloses:

An optical receiver as in claim 1, wherein the transimpedance amplifier circuit (Doh, transimpedance amplifier in paragraph [0003]; Kim, TIA in Fig. 1(b)) has a first frequency response (frequency response of some kind is inherent).

Regarding claim 7, Doh in view of Kim discloses:

A method for receiving an optical signal, comprising:

converting (Doh, e.g., 11 in Fig. 1) the optical signal into a corresponding current signal;

converting the corresponding current signal into a corresponding voltage signal with a transimpedance amplifier circuit (Kim, TIA in Fig. 1(b));

extracting clock information from the corresponding voltage signal (Doh, e.g., 15); and

regenerating the corresponding voltage signal to reduce jitter (Doh, regeneration of signal and suppression of jitter in paragraph [0002]).

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Doh in view of Kim.

Regarding claim 3, Doh in view of Kim does not expressly disclose:

An optical receiver as in claim 2, wherein the transimpedance amplifier circuit and the CDR circuit are formed on a single chip.

However, integration of circuitry is extremely well known in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to form these circuits of Doh on a single chip. One of ordinary skill in the art would have been motivated to do this for common benefits of

integration of circuits on a single chip, such as more compact size, economies of scale, and faster operation speeds.

Response to Arguments

7. Applicant's arguments filed on 22 November 2007 have been fully considered but they are not persuasive. Applicant presents two salient points.

Regarding the first point, Applicant provides an argument that the prior art of record does not teach coupling the TIA directly to the CDR circuit (REMARKS, p. 4-6). However, notice the newly applied teachings from Kim that address this limitation. Accordingly, this point is not persuasive.

Moreover, regarding claim 7, the language of claim 7 does not actually capture the subject matter of coupling the TIA directly to the CDR circuit. That is, notice the salient limitations of claim 7:

> "converting the corresponding current signal into a corresponding voltage signal with a transimpedance amplifier circuit;
>
> extracting clock information from the corresponding voltage signal".

The step of "extracting clock information from the corresponding voltage signal" is still disclosed by Doh. That is, the step of "converting the corresponding current signal into a corresponding voltage signal with a transimpedance amplifier circuit" is performed by the TIA 12 in Fig. 1 (Doh, paragraph [0003]). Limiting amplifier 13 in Fig. 1 provides level adjustment to this "corresponding voltage signal". Then, clock information is extracted from this "corresponding voltage signal" by CDR 15 in Fig. 1. Accordingly, Doh still discloses the limitations of claim 7.

Furthermore, even if the language of claim 7 is amended to capture the subject matter of coupling the TIA directly to the CDR circuit, there may be an issue under 35 U.S.C. 112, 2nd paragraph, regarding the clarity of claims 8 and 9. That is, claims 8 and 9 include a compensating step that would interpose the TIA and the step of "extracting clock information", i.e., the CDR circuit. Thus, this compensating step would conflict with any subject matter of coupling the TIA directly to the CDR circuit.

Regarding the second point, Applicant states:

> "Furthermore, with respect to the Examiner's rejection of claim 3, the Applicants disagree that it would be obvious to implement a transimpedance amplifier and a CDR circuit in the same integrated circuit package, or chip, at least because a limiting amplifier is normally interposed between the CDR circuit and the transimpedance amplifier, as taught by both Doh et al. and

> Swenson et al. Therefore, it would not be obvious to implement these circuits on a single chip merely because there are well known 'benefits of integration of circuits on a single chip', as contended by the Examiner. For this additional reason, the Applicants respectfully submit that claim 3 is patentable over Doh et al. and respectfully request that the rejection be withdrawn" (REMARKS, p. 7, last paragraph).

Examiner respectfully notes that the standing rejection of claim 3 under Doh in view of Kim does not incorporate a limiting amplifier between the CDR circuit and the transimpedance amplifier. Accordingly, this point is not persuasive.

Summarily, Applicant's arguments are not persuasive. Accordingly, Examiner respectfully maintains the standing rejections.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER